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SP	AJ	MOTA, M. et al.: "A flexible multi-channel high-resolution time-to-digital converter ASIC", 2000 IEEE Nuclear Science Symposium. Conference Record (Cat. No. OOCH37149), 2000 IEEE Nuclear Science Symposium. Conference Record, Lyon, France, 15-20 Oct. 2000, vol.2, pages 9/155-9 189, XP002236607 2000, Piscataway, NJ, USA, IEEE, USA ISBN: 0-7803-6503-8, page 9-155, page 9-158								
SP	AK	MOTA, M. et al: "A four-channel self-calibrating high-resolution time to digital converter" Electronics, Circuits and Systems, 1998, IEEE International Conference on Lisboa, Portugal 7-10 Sept. 1998, Piscataway, NJ, USA, IEEE, US, 7 Sept 1998 (1998-09-07), pages 409-412, XP010366204, ISBN: 0-7803-5008-1, page 409, page 410								
SP	AL	CHRISTIANSEN J.: "An integrated high resolution CMOS timing generator based on an array of delay locked loops", IEEE Journal of SolidoState Circuits, IEEE Inc. New York, US, vol. 31, no. 7, 1 July 1996 (1996-07-01), pages 952-957, XP000632381, ISSN: 0018-9200, the whole document								
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